m

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,266	05/20/2004	Dominik J. Schmidt	IVT.0033US	4584
21906 TROP PRI INE	7590 10/03/2007 P. & HII P.C		EXAMINER	
TROP PRUNER & HU, PC 1616 S. VOSS ROAD, SUITE 750			PHAN, DEAN	
HOUSTON, TX 77057-2631			ART UNIT	PAPER NUMBER
			2182	
			MAIL DATE	DELIVERY MODE
			10/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

## Advisory Action

Application No.	Applicant(s)	
10/690,266	SCHMIDT, DOMINIK J.	
Examiner	Art Unit	
	1	

Before the Filing of an Appeal Brief --The MAILING DATE of this communication appears on the cover sheet with the correspondence address --THE REPLY FILED 11 September 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. 1. 🔀 The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods: The period for reply expires months from the mailing date of the final rejection. b) 🔀 The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f). Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b). **NOTICE OF APPEAL** 2. The Notice of Appeal was filed on . A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a). **AMENDMENTS** 3. The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because (a) They raise new issues that would require further consideration and/or search (see NOTE below): (b) They raise the issue of new matter (see NOTE below); (c) They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal: and/or (d) They present additional claims without canceling a corresponding number of finally rejected claims. NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)). 4. The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324). 5. Applicant's reply has overcome the following rejection(s): 6. Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s). 7. 🛛 For purposes of appeal, the proposed amendment(s): a) 🗌 will not be entered, or b) 🖾 will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended. The status of the claim(s) is (or will be) as follows: Claim(s) allowed: Claim(s) objected to: Claim(s) rejected: Claim(s) withdrawn from consideration: \_\_\_\_\_. AFFIDAVIT OR OTHER EVIDENCE 8. The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e). 9. The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1). 10. The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached. REQUEST FOR RECONSIDERATION/OTHER 11. X The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see Attachment. 12. Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). 13. ☐ Other: . . SUPERVISORY PATENT EXAMINER

U.S. Patent and Trademark Office PTOL-303 (Rev. 08-06)

Application/Control Number: 10/690,266

Art Unit: 2182

## Response to Arguments

Applicant's arguments filed on 07/18/2007 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

- a. Prior art of record does not teach switching steps in claim 16.
- Prior art of record does not teach the second host processor family in reconfigurable processor core in claim 1.
- c. Prior art of record does not "suggest the combination of digital data multiplying circuit with the reconfigurable processor core"

In response to argument 'a', examiner respectfully traverses. It appears that the applicant is not interpreting the previous office action as intended by the examiner. Firstly, in figure 5, Schmidt discloses that the core 150 includes at least 3 processor family sets such as: CPUs, DSPs, ASICs. Also in paragraph 15, Schmidt discloses, "The reconfigurable processor core 150 can include one or more processors 151 such as MIPS processors and/or one or more digital signal processors (DSPs) 153, among others." A group of CPU, DSP, or ASIC processors is a processor family. Instructions execute with one of these processor families are a processor family instruction set. Therefore, the reconfigurable processor core can execute at least 3 processor family instruction sets. In this rejection, either DSP or ASIC instructions are considered the second processor family instruction set. The CPUs instructions are considered the first processor family instruction set, which is same as host processor 220 instructions since MIPS is a RISC microprocessor architecture.

Schmidt clearly discloses the step of "switching the system to process ... a second processor family instruction set" in paragraph 17, and further in paragraph 15, 31-32. Schmidt discloses, "These processors 151 and 153 can be configured to operate optimally on specific problems. For example, the bank of DSPs 153 can be optimized to handle discrete cosine transforms (DCTs) or Viterbi encodings, among others. Additionally, dedicated hardware 155 can be provided to handle specific algorithms in silicon more efficiently than the programmable processors 151 and 153. **The number of active processors is controlled depending on the application, so that power is not used when it is not needed.**" Note that "switching the system to process" is broad since the system includes any components. Therefore, by activating processors to control a certain application such as to handle discrete cosine transforms (DCTs), the system switches to process a first instruction of a second processor family instruction set. Also, since the processor 220 controls the reconfigurable processor core

Application/Control Number: 10/690,266 Page 3

Art Unit: 2182

100, by powering off active processors when it is not needed, the system switching to process a second instruction of the first processor family instruction set. Therefore, Schmidt discloses all the limitations in claim 16.

In response to argument 'b', examiner respectfully traverses. As explained above, the reconfigurable processor core 150 can include "MIPS processors **and**/or more DSPs". Therefore, Schmidt discloses the second host processor family in reconfigurable processor core.

In response to argument 'c', examiner respectfully traverses. Schmidt discloses a processor functions as a host (CPU 220), a reconfigurable processor core (wireless comm. 100), and processor type select circuit (par. 15). The only limitation that Schmidt does not teach is all elements are integrated in a single integrated circuit. Lee discloses the method that, by integrated in a single chip, it will greatly contribute to system miniaturization, low power consumption, and reduced cost. Therefore, it would have been obvious to one ordinary skill in the art at the time of invention to implement Schidmt's invention in a single integrated chip in order to obtain the above benefits.